IN THE CLAIMS:

Please amend the claims as follows:

1. (cancelled)

2. (Currently Amended) The method of ~~claim 1~~ claim 9 wherein the interruption is:

(a) another thread writing data read by the given program thread in the critical section, or

(b) another thread reading or writing data written by the given program thread.

3. (Currently Amended) The method of claim 2 wherein the interruption is detected by an invalidation of a cache block holding data of the critical section.

4. (Currently Amended) The method of ~~claim 1~~ claim 9 wherein absent the occurrence of a non cacheable operation limiting further speculation, the speculative execution is committed at the end of the critical section.

5. (Previously Presented) The method of claim 4 wherein the end of the critical section is detected by a pattern of instructions typically associated with a lock release.

6. (Previously Presented) The method of claim 5 wherein the pattern of instructions is a store instruction to a deduced lock variable address.

7. (Currently Amended) The method of ~~claim 1~~ claim 9 wherein absent the occurrence of a non cacheable operation limiting further speculation, the speculative execution is committed at a resource boundary limiting further speculation.

8. (Previously Presented) The method of claim 7 including the step of:

(d) if at step (c) there was no interruption from the execution of another thread acquiring a lock variable allowing the given thread to have exclusive access to the critical section and continuing execution from the commitment point to the conclusion of the critical section.

9. (Currently Amended) A method of coordinating access to common memory by multiple program threads comprising the steps of:

in each given program thread,

(a) detecting the beginning of a critical section of the given program thread in which interruption to access of the common memory could occur resulting from execution of other program threads;

(b) speculatively executing the critical section; and

(c) committing the speculative execution of the critical section if there has been no interruption to access of the common memory and squashing the speculative execution of the critical section if there has been an interruption~~The method of claim 1~~ wherein the speculative execution is committed upon the occurrence of a non cacheable operation limiting further speculation.

10. (Previously Presented) The method of claim 9 including the step of:

(d) if at step (c) there was no interruption from the execution of another thread acquiring a lock variable allowing the given thread to have exclusive access to the critical section and continuing execution from the commitment point to the conclusion of the critical section.

11. (Currently Amended) The method of ~~claim 1~~ claim 9 wherein step (a) includes reading of a lock variable and wherein step (b) is performed only when the lock variable is not held by another program thread.

12. (Currently Amended) The method of ~~claim 1~~ claim 9 wherein step (a) includes reading a prediction table holding historical data indicating past successes in speculatively executing the critical section and wherein step (b) is performed only when the prediction table indicates a likelihood of successful speculative execution of the critical section of above a predetermined threshold.

13. (Currently Amended) The method of ~~claim 1~~ claim 21 wherein step (a) deduces the beginning of a critical section by detecting patterns of instructions typically associated with a lock acquisitions.

14. (Previously Presented) The method of claim 13 wherein the pattern includes an atomic read/modify/write sequence.

15. (Currently Amended) The method of ~~claim 1~~ claim 9 wherein the critical section is preceded by a lock acquisition section and including the step of eliding the lock acquisition before step (b).

16. (Currently Amended) The method of ~~claim 1~~ claim 9 wherein the critical section ends with a lock release section and including the step of eliding the lock release section after step (c) when at step (c) upon reaching the end of the critical section, no interruption from the execution of another thread occurred.

17. (Currently Amended) The method of ~~claim 1~~ claim 9 including the further step of:

(d) after squashing the speculative execution of the critical section if there has been a interruption, re-executing the critical section speculatively.

18. (Previously Presented) The method of claim 17 wherein the speculative re-execution of the critical section is repeated up to a predetermined number of times until there is not a interruption.

19. (Currently Amended) The method of ~~claim 17~~ claim 18 wherein (d) if after the predetermined number of tries there remains a interruption from the execution of another thread, acquiring a lock variable allowing the given thread to have exclusive access to the critical section and continuing execution of the critical section from its beginning.

20. (Currently Amended) The method of ~~claim 1~~ claim 9 wherein the speculation executes the critical section using a cache memory to record the speculative execution without visibility to other processing units.

21. (Currently Amended) A method of coordinating access to common memory by multiple program threads comprising the steps of:

in each given program thread,

(a) detecting the beginning of a critical section of the given program thread in which interruption to access of the common memory could occur resulting from execution of other program threads;

(b) speculatively executing the critical section; and

(c) committing the speculative execution of the critical section if there has been no interruption to access of the common memory and squashing the speculative execution of the critical section if there has been an interruption ~~The method of claim 1~~ wherein the speculation executes the critical section eliding write instructions that do not change a value of memory location being written to.

22. (Cancelled)

23. (Currently Amended) ~~The lock elision circuit of claim 22~~ The method of claim 21 wherein the interfering access to the common memory is:

(a) another thread writing data read by the given program thread in the critical section, or

(b) another thread reading or writing data written by the given program thread.

24. (Currently Amended) ~~The lock elision circuit~~ The method of claim 23 wherein the computer architecture includes a cache and the ~~interfering access to the common memory~~ interruption is detected by an invalidation of a cache block holding data of the critical section.

25. (Currently Amended) ~~The lock elision circuit of claim 22~~ The method of claim 21 wherein the speculative execution is committed at the end of the critical section.

26. (Currently Amended) ~~The lock elision circuit of~~ The method of claim 25 wherein the end of the critical section is detected by a pattern of instructions typically associated with a lock release.

27. (Currently Amended) ~~The lock elision circuit~~ The method of claim 26 wherein the pattern of instructions is a store instruction to a deduced lock variable address.

28. (Currently Amended) ~~The lock elision circuit of claim 22~~ The method of claim 21 wherein the speculative execution is committed at a resource boundary limiting further speculation.

29. (Currently Amended) ~~The lock elision circuit~~ The method of claim 28 wherein when there is no interfering access to the common memory from the execution of another thread acquiring a lock variable, the lock elision circuit allows the given thread to have exclusive access to the critical section and continues execution from the commitment point to the conclusion of the critical section.

30. (Currently Amended) ~~The lock elision circuit of claim 22~~ The method of claim 21 wherein the lock elision circuit reads a lock variable and speculatively executes the critical section only when the lock variable is not held by another program thread.

31. (Currently Amended) ~~The lock elision circuit of claim 22~~ The method of claim 21 wherein the speculative execution is committed upon the occurrence of a non cacheable operation limiting further speculation.

32. (Currently Amended) ~~The lock elision circuit~~ The method of claim 31 including the step of:

(d) if at step (c) there was no interfering access to the common memory from the execution of another thread, acquiring a lock variable allowing the given thread to have exclusive access to the critical section and continuing execution from the commitment point to the conclusion of the critical section.

33. (Currently Amended) ~~The lock elision circuit of claim 22~~ The method of claim 21 including a prediction table holding historical data indicating past successes in speculatively executing the critical section and wherein the lock elision circuit speculatively executes the critical section only when the prediction table indicates a likelihood of successful speculative execution of the critical section of above a predetermined threshold.

34. (Currently Amended) ~~The lock elision circuit of claim 22~~ The method of claim 21 wherein the lock elision circuit determines the beginning of a critical section by detecting patterns of instructions typically associated with a lock acquisitions.

35. (Currently Amended) ~~The lock elision circuit~~ The method of claim 34 wherein the pattern includes an atomic read/modify/write sequence.

36. (Currently Amended) ~~The lock elision circuit of claim 22~~ The method of claim 21 wherein the critical section is preceded by a lock acquisition section and wherein the lock elision circuit elides the lock acquisition before speculation.

37. (Currently Amended) ~~The lock elision circuit of claim 22~~ The method of claim 21 wherein the critical section ends with a lock release section and wherein the lock elision circuit elides the lock release section after speculation when upon reaching the end of the critical section, no interfering access to the common memory from the execution of another thread occurred.

38. (Currently Amended) ~~The lock elision circuit of claim 22~~ The method of claim 21 wherein after squashing the speculative execution of the critical section, if there has been an interfering access to the common memory, the lock elision circuit re-executes the critical section speculatively.

39. (Currently Amended) ~~The lock elision circuit~~ The method of claim 38 wherein the lock elision circuit repeats the speculative re-execution of the critical section up to a predetermined number of times until there is not an interfering access to the common memory.

40. (Currently Amended) ~~The lock elision circuit~~ The method of claim 39 wherein if after the predetermined number of tries there remains an interfering access to the common memory from the execution of another thread, the lock elision circuit allows acquisition of a lock variable allowing the given thread to have exclusive access to the critical section and continuing execution of the critical section from its beginning.

41. (Currently Amended) ~~The lock elision circuit of claim 22~~ The method of claim 21 wherein the computer architecture includes a cache memory and the lock elision circuit uses the cache memory to record the speculative execution without visibility to other processing units.

42. (Currently Amended) ~~The lock elision circuit of claim 22~~ The method of claim 21 wherein the lock elision circuit elides write instructions within the critical section that do not change a value of memory location being written to.

43.-47 (Cancelled)

48. (New) The method of claim 21 wherein the value in memory subject to the elided write instruction is a lock variable for controlling access to the critical section by competing program threads.

49. (New) The method of claim 21 wherein step (a) deduces the beginning of a critical section by detecting special delimiter instructions.

50. (New) The method of claim 9 wherein step (a) deduces the beginning of a critical section by detecting special delimiter instructions.